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METHOD FOR SEPARATING AND FORMING ELEMENTS OF SEMICONDUCTOR DEVICE
[Handotai Sochi No Shoshi Bunri Keisei Hoho]

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Specification /1[1]

1. Title of the Invention: METHOD FOR SEPARATING AND FORMING ELEMENTS OF SEMICONDUCTOR DEVICE

2. Claims

1. A method for separating and forming elements of a semiconductor device characterized by the fact that it includes a process for forming an insulating film on the surface of a semiconductor, a process for forming a polycrystalline silicon film on the above-mentioned insulating film, a process for forming a first silicon nitride film on the above-mentioned polycrystalline silicon film, a process for selectively etching the above-mentioned first silicon nitride film, the above-mentioned polycrystalline silicon film, the above-mentioned insulating film, and a semiconductor substrate, a process for laminating a second silicon nitride film, a process for anisotropicaly etching the above-mentioned second silicon nitride film and forming a spacer of the above-mentioned second silicon nitride film at the side wall of the above-mentioned polycrystalline silicon film, a process for oxidizing an area, which is not covered with the polycrystalline silicon film, using the above-mentioned polycrystalline silicon film separated from the above-mentioned first silicon nitride film and the above-mentioned second silicon nitride film as an oxidizing mask, and a

[1]Numbers in the margin indicate pagination in the foreign text.

process for forming an area covered with the oxide film and an area, which is not covered with the oxide film, by sequentially removing the oxide film on the above-mentioned first and second silicon nitride films, the above-mentioned first and second silicon nitride film, the above-mentioned polycrystalline silicon film, and the above-mentioned insulating film.

2. The method for separating and forming elements of a semiconductor device of Claim 1 characterized by the fact that the semiconductor is silicon.

3. The method for separating and forming elements of a semiconductor device of Claim 1 characterized by the fact that the insulating film being formed on the semiconductor surface is a silicon nitride film of 30-1000 Å.

4. The method for separating and forming elements of a semiconductor device of Claim 1 characterized by the fact that the polycrystalline silicon film has a film thickness of 300-6000 Å.

5. The method for separating and forming elements of a semiconductor device of Claim 1 characterized by the fact that the thickness of the first silicon nitride film is 300-2000 Å.

6. The method for separating and forming elements of a semiconductor device of Claim 1 characterized by the fact that the amount of semiconductor substrate etched is in a range of 0.4-0.6 of the thickness of an oxide film for separating elements. /2

7. The method for separating and forming elements of a

semiconductor device of Claim 1 characterized by the fact that the thickness of the second silicon nitride film is 300-3000 Å.

3. Detailed explanation of the invention

(Industrial application fields of the invention)

The present invention pertains to a method for separating and forming elements of a semiconductor device.

(Outline of the invention)

The present invention pertains to a method for separating and forming elements without a small buzz peak and little defects. After a thin oxide film is formed on the surface of a semiconductor, a polycrystalline silicon film is deposited, and a silicon nitride film is laminated. Next, the silicon nitride film, polycrystalline silicon film, silicon oxide film, and semiconductor substrate of the part being a future element separating area are selectively etched.

Next, a silicon nitride film is laminated, and the silicon nitride film is anisotropically etched using an anisotropic etching method such as reactive dry etching, and the silicon oxide film is made to remain at the side wall and the upper part of the polycrystalline silicon film. Then, the silicon nitride film of the other areas is completely removed. Using the polycrystalline silicon film covered with the silicon nitride film as a mask, the area having no polycrystalline silicon film is oxidized, and an element separating area is formed. Next, the nitride film, polycrystalline silicon film, and oxide film

existing at the part being an active area are sequentially removed.

Thus, the element separating area covered with a thick oxide film and the active area, to which the semiconductor surface is exposed, are formed. Thereafter, semiconductor elements are prepared in the active area.

(Prior art)

In the element separation of the semiconductor elements, a selective oxidizing method (LOCOS method) has been used. The LOCOS method is as follows. As shown in Figure 3(a), a semiconductor surface 11 of silicon, etc., is oxidized, and a relaxing silicon oxide film 12 for relaxing a stress being generated during the selective oxidation is formed. Furthermore, a silicon nitride film 13 as a material for an oxidation mask during the selective oxidation is laminated by a CVD method. Next, as shown in Figure 2(b), a resist 14 is formed in a desired shape using a photoetching method, and using the resist 14 as a mask, the silicon oxide film 13 is etched. Furthermore, if oxidation is carried out as shown in Figure 2(c), the area having no silicon oxide film is oxidized, and a thick oxide film 15 for an element separation is formed. On the other hand, the area, which is not covered with the silicon nitride film 13, is not oxidized. Next, as shown in Figure 2(d), an element separating area 16 and an active area 17 are formed by sequentially removing the silicon nitride film and the relaxing silicon oxide film. Then, semiconductor elements are formed in the active area 17.

(Problem to be solved by the invention)

In the conventional LOCOS method, as shown in Figure 2(d), the oxide film with a length of l is stretched in a slender shape from the boundary of the element separating area to the active area, so that the active area is narrowed (this is called a buzz peak). The length l of the buzz peak depends on oxidation conditions, etc., however it is usually 0.5 μm or more. The element molecule [sic; separating] area cannot be narrowed. As a method for reducing the buzz peak, the relaxing silicon oxide film is thinned, or the silicon nitride film is thickened. However, in any cases, a large stress is exerted on the semiconductor substrate in the LOCOS oxidizing process, and many crystal defects are generated, so that the element separating characteristic is deteriorated. Therefore, in the conventional LOCOS method, the above-mentioned buzz peak cannot be reduced while maintaining a favorable element separating characteristic.

(Mechanism for solving the problems)

In order to solve the above-mentioned problems, in the present invention, the side surface and the surface of a polycrystalline silicon film having about the same thermal expansion coefficient as that of a semiconductor substrate (silicon) are covered with a silicon nitride film, and using the polycrystalline silicon film as an oxidizing mask, the area, which is not covered with the polycrystalline silicon film, is oxidized. Also, the semiconductor substrate of the area, which is not covered with the polycrystalline silicon film, is etched

to some degree, that is, at an amount corresponding to the thickness of about half of the thick LOCOS oxide film prior to the oxidation.

(Operation)

Since the polycrystalline silicon film with a thermal expansion coefficient equal to that of the silicon substrate is used as an oxidizing mask for the side wall silicon nitride film, the buzz peak is small, and elements with little defects can be separated. Also, since the semiconductor substrate is etched at a corresponding amount prior to the LOCOS oxidation, the level difference of the element separating area and the active area can be reduced. /3

(Application examples)

The application example of the present invention is shown in Figures 1(a)-(g). As shown in Figure 1(a), an insulating film 2 is laminated on a semiconductor substrate 1 such as silicon (Si). Needless to say, the semiconductor substrate 1 may also be semiconductor substrates other than silicon. For example, compound semiconductors such as gallium arsenic (GaAs) and indium phosphorus (InP) may also be used. Also, the insulating film 2 is generally a silicon oxide film, and it can be deposited by oxidizing method, chemical vapor deposition (CVD) method, or physical vapor deposition (PVD) method. The silicon oxide film 2 is also called a [illegible] (pad) oxide film and has a function of relaxing a stress being generated in the semiconductor substrate during a field oxidation of the postprocess. In the

selective oxidation (LOCOS) method, there is a tendency that the thicker the silicon oxide film 2, the longer the buzz peak. On the contrary, the thinner the silicon oxide film, the shorter the buzz peak, however the defect density is increased in the semiconductor substrate. Next, a polycrystalline silicon film 3 is deposited on the silicon oxide film 2. A silicon nitride film 4 is further laminated on the polycrystalline silicon film 3. The polycrystalline silicon film 3 can be laminated by the CVD method or PVD method. In the CVD method, the polycrystalline silicon film 3 is formed by a chemical vapor deposition using a silane group gas (Si_mN_n) such as silane gas (SiN_4) or disilane gas (Si_2N_6), or trisilane (Si_3N_8). Also, the silicon nitride film 4 can be laminated by the CVD method or PVD method. In the CVD method, the silicon nitride film 4 is formed by a reaction of dichlorsilane gas (SiN_2Cl_2) and an ammonia gas (NH_3) or a reaction of a silane gas (SiN_4) and an ammonia gas (NH_3). Next, as shown in Figure 1(b), the above-mentioned silicon nitride film 4, polycrystalline silicon film 3, and silicon oxide film 2 are selectively etched using photoetching method, etc. In other words, the silicon nitride film 4, polycrystalline silicon film 3, and silicon oxide film 3 being an element separating area are removed by etching. The etching may be wet methods, however dry methods with little [illegible] etching are more preferable. Of the dry methods, in particular, a reactive ion etching (usually called a RIE) with a large anisotropy and a plasma etching (usually called a PPE) are preferable. In preparing a fine

pattern of 3 μ or less, the anisotropic etching is especially required. Also, since the silicon oxide film 2 is generally as thin as 500 Å or less, there is no special problem in etching using the wet method. The silicon nitride film 4, polycrystalline silicon film 3, and silicon oxide film may also be etched by separate etching apparatuses, and they may also be continuously etched using the same etching apparatus. The part, in which the silicon nitride film 4 and the polycrystalline silicon film 3 are removed by etching, will be an active area. Next, as shown in Figure 1(c), thin films such as silicon nitride film 4 are removed, and the semiconductor substrate of the part, to which the semiconductor substrate 1 such as silicon is exposed, is etched. The purpose of etching of the semiconductor substrate is to reduce the level difference of the active area and the element separating area being generated after the selective oxidation and to reduce defects in the semiconductor substrate. In etching the semiconductor substrate 1, needless to say, a mask material such as resist existing on the silicon nitride film 4 of the part to be an active area may be present.

However, in case a heat treatment process such as oxidation is adopted between Figures 1(b) and (c), the mask material such as resist must be removed. As the silicon etching method in Figure 1(c), there are wet methods and dry methods. In the wet methods, an etching solution for anisotropically etching the semiconductor substrate such as silicon is preferable. For example, the anisotropic etching is enabled by etching with an

alkali solution such as potassium hydroxide.

Also, in the dry methods, in particular, the RIE and PPE, which can be anisotropically etched, are used. The amount of semiconductor substrate such as silicon etched is an amount selected so that the active area and the element separating area are flat at a time of the selective oxidation. For example, in case the semiconductor substrate 1 is silicon, if the thickness of a field oxide film of the element separating area is 6000 Å, the amount of silicon substrate being etched is about 3000 Å.

Next, as shown in Figure 1(d), a second silicon nitride film 6 is laminated. The nitride film 6 can also be formed by the CVD method or PVD method similarly to the nitride film 4.

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Next, using a dry etching method (RIE, or PPE, or ion sealing, or sputtering etching method) with a strong anisotropy, the second silicon oxide film 6 is etched on the entire surface. At that time, the nitride film of the part being the element separating area is preferably completely removed by etching. The silicon nitride film 6 of the flat part is all etched by the anisotropic etching, however since the thickness of the silicon nitride film 6 of the side wall part of the polycrystalline silicon film 3 is thick, the silicon nitride film 6 remains as a spacer at the side wall of the polycrystalline silicon film 3. This pattern is shown in Figure 1(e).

Next, a thick oxide film 7 is deposited on the areas other than a certain part of the polycrystalline silicon film 3 covered

with the nitride film by oxidizing an oxidizing atmosphere as shown in Figure 1(f), however in the certain area of the polycrystalline silicon film covered with the nitride film, since the nitride film is an oxidizing mask, the oxide film is not deposited. In particular, the second nitride film 6 remaining as a spacer prevents the oxidation in the horizontal direction. Thus, the buzz peak, which is a horizontal oxidation, is extremely reduced. Then, the thin oxide film deposited on the nitride film during the oxidation, silicon nitride films 6 and 4, polycrystalline silicon film 3, and relaxing oxide film 2 are sequentially removed, and as shown in Figure 1(g), an active (element) area 8 and an element separating area 9 are formed. Thereafter, [illegible] elements such as transistor are formed in the active area 8, and an IC is prepared.

As shown in Figures 1(a)-(g), after the process shown in Figure 1(c), or the process shown in Figure 1(d), or the process shown in Figure 1(e), an ion implantation for preventing a field area inversion may also be carried out.

Since the polycrystalline silicon film 3 has the same composition as that of the silicon which is the semiconductor substrate, the physical properties are similar. During the selective oxidation shown in Figure 1(f), if the difference in the thermal expansion coefficient between the oxidizing mask and the substrate material is large, defects are apt to be generated in the semiconductor substrate, however in the present invention, since the polycrystalline silicon film is used as a main material

of the oxidizing mask, the calorie is small, and defects are difficult to be generated in the semiconductor substrate 1. Also, owing to the side wall silicon nitride film, the horizontal oxidation is seldom caused, and an element separating area without a small buzz peak is formed. Furthermore, the relaxing silicon oxide film 2 can be more thinned, compared with conventional films, so that the reduction of the buzz peak can also be expected.

In an ordinary LOCOS method, the thickness of the relaxing silicon oxide film 2 is 500-1000 Å, however if the present invention is used, the thickness can be reduced to 30-1000 Å. Also, the thicker the thickness of the polycrystalline silicon film 3, the smaller the buzz peak, however 300-6000 Å is practically preferable. Also, the thickness of the silicon nitride film 4 may have a thickness that remains sufficiently even by an overetching of the silicon nitride film 6 and a thickness that the polycrystalline silicon film 3 is not oxidized during a field oxidation. Furthermore, the thicker the thickness of the silicon nitride film 6, the thicker the thickness of the side wall, and the buzz peak is reduced. However, 300-1000 Å is practically preferable. As an example, when the relaxing silicon oxide film 2, polycrystalline silicon film 3, silicon nitride film 6, the silicon etching with KOH, and field oxide film 7 are respectively deposited at 200 Å, 4000 Å, 1500 Å, 1500 Å, 3000 Å, and 6000 Å, the buzz peak is 0.2 μ or less, and the active area and the element separating area with almost the same pattern size

can be formed. Also, the level difference of the active area and the element separating area is 500 Å or less, and a favorable flatness is also obtained. Furthermore, at that time, the defect density is very small, and about the same favorable element separating characteristic as that of the conventional LOCOS method is exhibited.

(Effects of the invention)

As explained above, according to the present invention, a favorable element separation with little defects and a very small buzz peak can be realized by a selective oxidation using a polycrystalline silicon film, whose surface and side wall are covered with a silicon nitride film, as an oxidizing mask.

4. Brief description of the figures

Figures 1(a)-(g) are cross sections showing the process sequence of the manufacturing method of the present invention. Figures 2(a)-(d) are cross section showing the process sequence of a conventional manufacturing method.

1, 11 Semiconductor substrates

2, 12 Silicon oxide films

/5

3 Polycrystalline silicon film

4, 13 (First) silicon nitride films

6 (Second) silicon nitride film

7, 15 Silicon oxide films (field oxide film)

14	Resist
8, 17	Active areas
9, 16	Element separating areas

Keys to Figures 1 and 2:

Figure 1: Cross sections showing the process sequence of the manufacturing method of the present invention

(a)

1	Semiconductor substrate
2	Silicon oxide film
3	Polycrystalline silicon film
4	Silicon nitride film

(c)

A.	Silicon etching

(d)

6	Silicon nitride film

(f)

7	Silicon oxide film
8	Active area
9	Element separating area

Figure 2: Cross sections showing the process sequence of a conventional manufacturing method

3・・・・・多結晶シリコン膜
4，13・・・（第1の）シリコン窒化膜
6・・・・・（第2　）シリコン窒化膜
7，15・・・シリコン酸化膜（フィールド酸化膜）
14・・・・・レジスト
7，17・・・活性領域
8，16・・・素子分離領域

以　上

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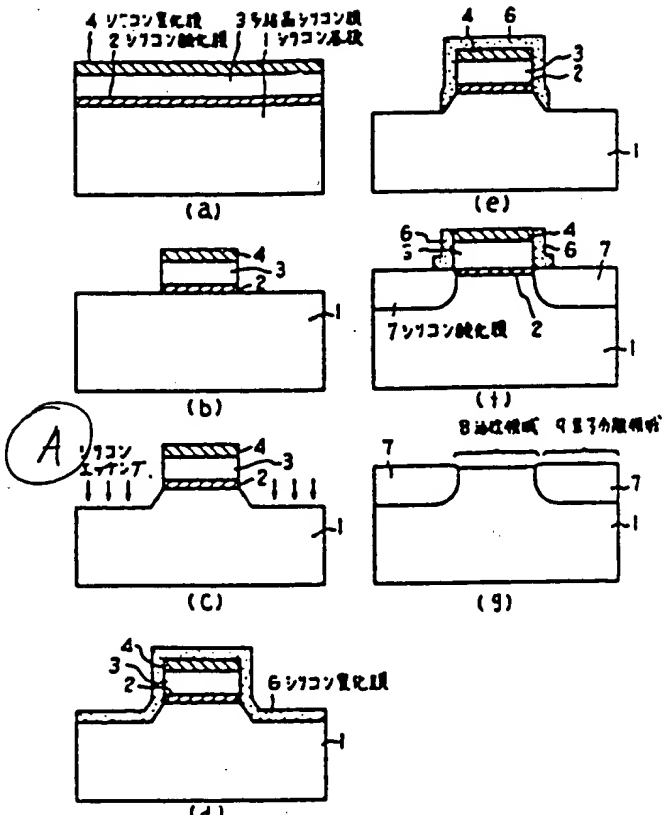
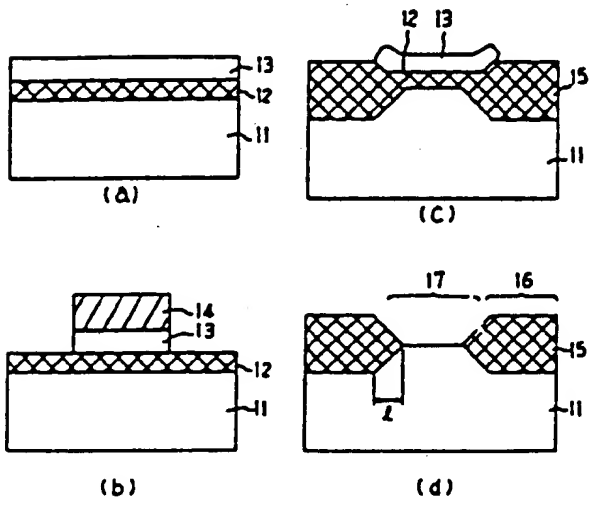
代理人　弁理士　最　上　　務（他1名）



本発明の素子分離形成方法の工程順を示す断面図
第1図



従来の素子分離方法の工程順を示す断面図
第2図

applicant's copy

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FORMATION OF ELEMENT ISOLATION OF SEMICONDUCTOR DEVICE

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ABSTRACT:

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FORMATION OF ELEMENT ISOLATION OF SEMICONDUCTOR DEVICE

PURPOSE:To realize element isolation excellent in characteristics by a method wherein a polycrystalline silicon film covered by a silicon nitride film on its surface and sides serves as a mask in a selective oxidation process.

CONSTITUTION:A silicon oxide film 2, polycrystalline silicon film 3, and silicon nitride film 4 are formed on a silicon semiconductor substrate 1, and are locally subjected to selective etching, together with the silicon semiconductor substrate 1, for an element isolating region 9 to be created in a later process. A silicon nitride film 6 is formed and then removed by anisotropic etching, with a portion thereof retained on the sides and top of the polycrystalline silicon film 3. The polycrystalline silicon film 3 covered by a silicon nitride film 6 serves as a mask in a process for the
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FORMATION OF ELEMENT ISOLATION OF SEMICONDUCTOR DEVICE

oxidation of the region free of the polycrystalline silicon film 3 into an element isolating region 9. Isolation realizes containing less defects.

=>

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⑭発明の名称　半導体装置の素子分離形成方法

⑳特　願　昭62-105372

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明　細　書

1．発明の名称

半導体装置の素子分離形成方法

2．特許請求の範囲

(1)半導体表面に絶縁膜を形成する工程と、前記絶縁膜上に多結晶シリコン膜を形成する工程と、前記多結晶シリコン膜上に第1のシリコン窒化膜を形成する工程と、前記第1のシリコン窒化膜と前記多結晶シリコン膜と前記絶縁膜と半導体基板を選択的に順次エッチングする工程と、第2のシリコン窒化膜を積層する工程と、前記第2のシリコン窒化膜を異方性エッチングし前記多結晶シリコン膜の側壁に前記第2のシリコン窒化膜のスペーサを形成する工程と、前記第1のシリコン窒化膜および前記第2のシリコン窒化膜から成れた前記多結晶シリコン膜を酸化マスクとして多結晶シリコン膜で被れていない領域を酸化する工程と、前記第1および第2のシリコン窒化膜上の酸化膜と前記第1および第2のシリコン窒化膜と多結晶シリコン膜と前記絶縁膜とを順次除去する事により、酸化膜で被れた領域と酸化膜のない領域を形成する工程と、を含む事を特徴とする半導体装置の素子分離形成方法。

(2)半導体はシリコンである事を特徴とする特許請求の範囲第1項記載の半導体装置の素子分離形成方法。

(3)半導体表面に形成する絶縁膜30～1000Åのシリコン酸化膜である事を特徴とする特許請求の範囲第1項記載の半導体装置の素子分離形成方法。

(4)多結晶シリコン膜は300～6000Åの膜厚を有する事を特徴とする特許請求の範囲第1項記載の半導体装置の素子分離形成方法。

(5)第1のシリコン窒化膜の厚みは300～2000Åである事を特徴とする特許請求の範囲第1項記載半導体装置の素子分離形成方法。

(6)半導体基板のエッチング量は素子分離用酸化膜の厚みの0.4～0.6の間にある事を　徴とする許請求の範囲第1項記載の半導体装置　素子分離形成方法。

(3)第2のシリコン窒化膜の厚みは300～3000Åである事を特徴とする　特許請求の範囲第1項記載の半導体装置の素子分離形成方法。

3．発明の詳細な説明

〔産業上の利用分野〕

この発明は、半導体装置の素子分離形成方法に関する。

〔発明の概要〕

この発明は、バーズビークが小さく欠陥の少ない素子分離形成方法に関するもので、半導体表面に薄い酸化膜を形成した後、多結晶シリコン膜を成長させ、さらにシリコン窒化膜を積層させる。次に将来素子分離領域となる部分のシリコン窒化膜、多結晶シリコン膜、シリコン酸化膜および半導体基板を選択的にエッチングする。

次に、シリコン窒化膜を積層し、反応性ドライエッチング等の異方性エッチング法を用い、このシリコン窒化膜を異方性エッチングし、多結晶シリコン膜の側壁と上部とにシリコン窒化膜を残し、他の領域　シリコン窒化膜を完全に除去する。このシリコン窒化膜で被れた多結晶シリコン膜をマスクにして、多結晶シリコン膜のない領域を酸化し素子分離領域を形成する。次に活性領域となる部分に存在する窒化膜、多結晶シリコン膜および酸化膜を順次除去する。

以上により厚い酸化膜で被れた素子分離領域と半導体表面が露出している活性領域が形成される。この後、活性領域には半導体素子が作成される。

〔従来の技術〕

半導体素子の素子分離とて従来から選択酸化法（ＬＯＣＯＳ法）が使用されている。このＬＯＣＯＳ法は次の様なものである。第2図(a)に示す様にシリコンなどの半導体表面11を酸化し選択酸化時に発生する応力を緩和するための緩衝用シリコン酸化膜12を形成し、さらに選択酸化時の酸化マスク用材料としてのシリコン窒化膜13をＣＶＤ法にて積層する。次に第2図(b)に示す様に写真食刻法を用いレジスト14を所望の形状に形成し、このレジス14をマスクとしてシリコン窒化膜13をエッチングする。さらに第2図(c)に示す様に酸化を行うとシリコン窒化膜のない領域は酸化され厚い素子分離用の酸化膜15が形成され、一方シリコン窒化膜13で被れていない領域は殆ど酸化されない。次に第2図(d)に示す様にシリコン窒化膜および緩衝用シリコン酸化膜を順次エッチング除去する事により、素子分離領域16と活性領域17が完成する。この後、活性領域17には半導体素子が形成される。

〔発明が解決しようとする問題点〕

従来のＬＯＣＯＳ法では第2図(d)に示す様に素子分離領域の境界から活性領域へ長さℓの酸化膜が細長く伸び、活性領域を狭くしてしまう。（これをバーズ・ビークという）このバーズ・ビークの長さℓは酸化条件等によっても異なるが、通常は0.5μm以上あり、素子分子領域も狭くする事ができない。このバーズ・ビークを小さくする方法として、緩衝用シリコン酸化膜を薄くするかあるいはシリコン窒化膜を厚くする方法があるが、どちらの場合もＬＯＣＯＳ酸化工程で半導体基板に大きな応力を及ぼし多数の結晶欠陥を誘起してしまい、素子、分離特性を劣化させる。従って良好な素子分離特性を保持しながら、上記のバーズ・ビークを小さくする事は、従来のＬＯＣＯＳ法を用いて不可能である。

〔問題点を解決するための手段〕

上記問題点を解決するためにこの発明は、半導体基板（シリコン）と同程度の熱膨張係数を持つ多結晶シリコン膜の側面と表面をシリコン窒化膜で被い、この多結晶シリコン膜を酸化マスクとして、多結晶シリコン膜で被れていない領域を酸化する。また、多結晶シリコン膜で被れていない領域の半導体基板を酸化前に、ある程度つまり厚いＬＯＣＯＳ酸化膜の膜ね半分の厚みに相当する量をエッチングしておく。

〔作用〕

シリコン基板と熱膨張係数の等しい多結晶シリコン膜を側壁シリコン窒化膜を酸化マスクとして使用しているから、バーズ・ビークが小さく欠陥の少ない素子分離が可能となる。またＬＯＣＯＳ酸化前に半導体基板を相当量エッチングしている

ため、素子分離領域と活性領域の段差を小さくする事ができる。

〔実施例〕

本発明の実施例を第1図(a)～(d)に示す。第1図(a)に示す様にシリコン(Si)などの半導体基板1の上に絶縁膜2を積層する。この半導体基板1はもちろんシリコン以外の半導体基板でもよい。例えば、砒化ガリウム(GaAs)インジウムリン(I。P)等の化合物半導体でもよい。また絶縁膜2は一般にはシリコン酸化膜であり、酸化法でも化学気相成長（ＣＶＤ）法でも物理成長法（ＰＶＤ）でも成長できる。このシリコン酸化膜2は緩衝（バッファ）酸化膜とも言われ、後工程のフィールド酸化の時に半導体基板中に誘発する応力を緩和する働きを持っている。選択酸化（ＬＯＣＯＳ）法においてこのシリコン酸化膜2が厚いほどバーズビークは長くなる傾向にある。逆にシリコン酸化膜2が薄いほどバーズビークは短くなるが、一方で半導体基板中に欠陥密度が多くなる。次にシリコン酸化膜2の上に多結晶シリコン膜3を成長させる。この多結晶シリコン膜3の上にさらにシリコン窒化膜4を積層する。多結晶シリコン膜3はＣＶＤ法でもＰＶＤ法でも積層する事ができる。ＣＶＤ法の場合多結晶シリコン膜3はシランガス(SiH_4)またはジシランガス(Si_2H_6)またはトリシラン(Si_3H_8)等のシラン系ガス(Si_nH_m) を用いた化学気相成長で形成される。またシリコン窒化膜4もＣＶＤ法でもＰＶＤ法でも積層する事ができる。ＣＶＤ法の場合、シリコン窒化膜4はジクロルシランガス(SiH_2Cl_2)とアンモニアガス(NH_3)との反応により、またはシランガス(SiH_4)とアンモニアガス(NH_3)との反応により形成される。次に第1図(b)に示す様に、上記のシリコン窒化膜4と多結晶シリコン膜3とシリコン酸化膜2を写真食刻法等の方法を用いて選択的にエッチング除去する。すなわち、素子分離領域となる部分のシリコン窒化膜4および多結晶シリコン膜3およびシリコン酸化膜2をエッチング除去する。このエッチングは湿式法でも良いがサイドエッチングの少ない乾式法がより良い。乾式法の中で特に異方性の大きい反応性イオンエッチング（通称ＲＩＥ）やプラズマエッチング（通称ＰＰＥ）が好ましい。３ミクロン以下の微細なパターンを作成するにはこの異方性エッチングが特に必要となる。また、シリコン酸化膜2は一般には５００Ａ以下と薄いので湿式法でエッチングしても特に問題はない。シリコン窒化膜4と多結晶シリコン膜3とシリコン酸化膜2とを別々のエッチング装置でエッチングしても良いし、同一のエッチング装置を用いて連続的にエッチングしても良い。シリコン窒化膜4と多結晶シリコン膜3をエッチング除去しない部分は将来活性領域となる。次に第1図(c)に示す様にシリコン窒化膜4等の酸膜が除去され、シリコン等の半導体基板1の露出した部分の半導体基板をエッチングする。この半導体基板のエッチングの目的は選択酸化を行った後に発生する活性領域と素子分離領域との段差を小さくする事とバーズビークを少なくする事および半導体基板中の欠陥を低減する事である。この半導体基板1のエッチングに際し、活性領域となるべき部分のシリコン窒化膜4の上に存在するレジスト等のマスク材料はあっても良い事はもちろんである。

ただ、第1図(b)と(c)との間に酸化等の熱処理工程が入る場合はレジスト等のマスク材料は除去されねばならない。第1図(c)におけるシリコンエッチングの方法として、湿式法と乾式法がある。湿式法の場合、シリコン等の半導体基板を異方的にエッチングするエッチング液が望ましい。たとえば、水酸化カリウム等のアルカリ液でエッチングする事により異方的にエッチングできる。

また、乾式法の場合、特に異方性エッチング可能なＲＩＥやＰＰＥが用いられる。シリコン等の半導体基板1をエッチングする量は、将来選択酸化した時に活性領域と素子分離領域とが平坦になる様に選ばれた量である。例えば半導体基板1がシリコンの場合、素子分離領域のフィールド酸化膜の厚みが6000Åならば、シリコン基板をエッチングする量は約3000Åとなる。

次に第1図(d)に示す様に、第2のシリコン窒化膜6を積層する。この窒化膜6も窒化膜4と同様

にCVD法またはPVD法等の方法により形成できる。次に異方性の強いドライエッチング法（RIEまたはPPEまたはイオンシリング、またはスパッタエッチング等の方法）を用いて第2のシリコン窒化膜6を全面エッチングする。この時素子分離領域となる部分の窒化膜は完全にエッチング除去する事が望ましい。この異方性エッチングより平坦部のシリコン窒化膜6はすべてエッチングされるが、多結晶シリコン膜3の側壁部分のシリコン窒化膜6の厚みは厚いので、多結晶シリコン膜3の側壁にシリコン窒化膜6はスペーサーとして残っている。この様子は第1図(c)に示されている。

次に酸化雰囲気の中で酸化を行うと第1図(d)に示す様に、窒化膜で被れた多結晶シリコン膜3がある部分以外の領域には厚い酸化膜7が成長するが、窒化膜で被れた多結晶シリコン膜のある領域は窒化膜が酸化マスクとなる為、酸化膜は成長しない。特にスペーサーとして残っている第2の窒化膜6は横方向への酸化を防止する。これにより膜のために横方向酸化は殆ど起こらず、バーズビークの小さい素子分離が形成される。さらに素子用シリコン酸化膜2も従来より薄くする事ができ、これによるバーズビークの減少も期待できる。

通常のLOCOS法では素子用シリコン酸化膜2の厚みは500～1000Åであるが、本発明を用いると30～1000Åの厚みにできる。また多結晶シリコン膜3の厚みは厚いほどバーズビークが小さくなるが、実用上300～6000Åが好ましい。またシリコン窒化膜4の厚みはシリコン窒化膜6のオーバーエッチングしても充分残っているだけの厚みとかつフィールド酸化時に多結晶シリコン膜3が酸化しないだけの厚みとを有していればよい。さらにシリコン窒化膜6の厚みも厚いほど側壁の厚みも厚くなりバーズビークを小さくする。しかし実用的には300～3000Åが好ましい。一例として、素子用シリコン酸化膜2を200Å、多結晶シリコン膜3を4000Å、シリコン窒化膜4を1500Å、シリコン窒化膜6を1500Å、シリコンエッチングをKOHで3000Å行い、フィールド酸化膜7を6000Å成長させた時のバーズビークは0.2μ以下となり、ほぼパターン寸法通りの活性領域と素子分離領域ができる。また活性領域と素子分離領域の段差は500Å以下となり良好な平坦性も得られている。さらにこの時の欠陥密度も非常に小さく、従来のLOCOS法と同程度の良好な素子分離特性を示した。

〔発明の効果〕

この発明は以上説明したように、シリコン窒化膜で表面および側壁を被れた多結晶シリコン膜を酸化マスクとして選択酸化する事により、欠陥も少なく、バーズビークも非常に小さい良好な素子分離を実現できる。

4．図面の簡単な説明

第1図(a)～(d)はこの発明の製造方法の工程順を示す断面図、第2図(a)～(d)は従来の製造方法の工程順を示す断面図である。

1，11・・・半導体基板

2，12・・・シリコン酸化膜

3・・・・・多結晶シリコン膜

4，13・・・（第1の）シリコン窒化膜

6・・・・・（第2の）シリコン窒化膜

7，15・・・シリコン酸化膜（フィールド酸化膜）

14・・・・・レジスト

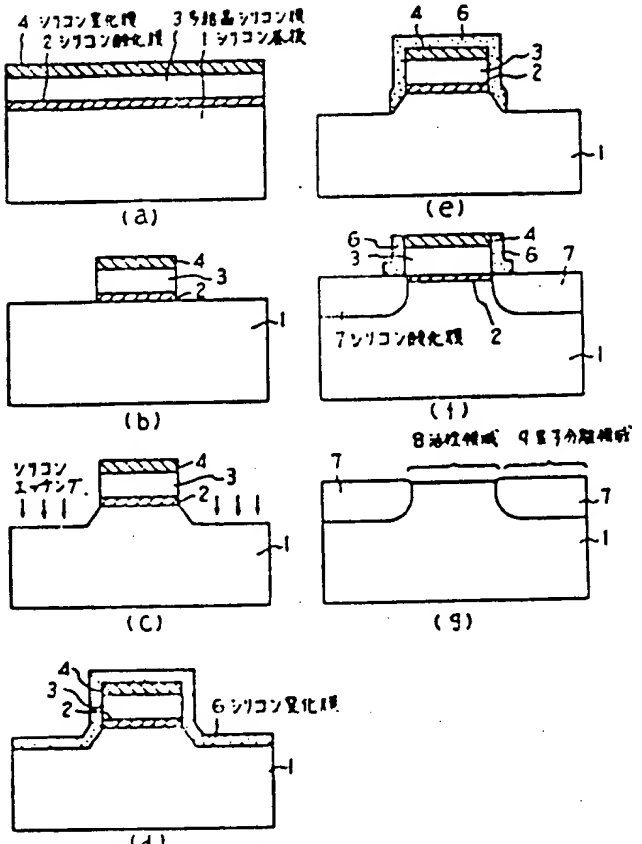
7，17・・・活性領域

8，16・・・素子分離領域

以　上

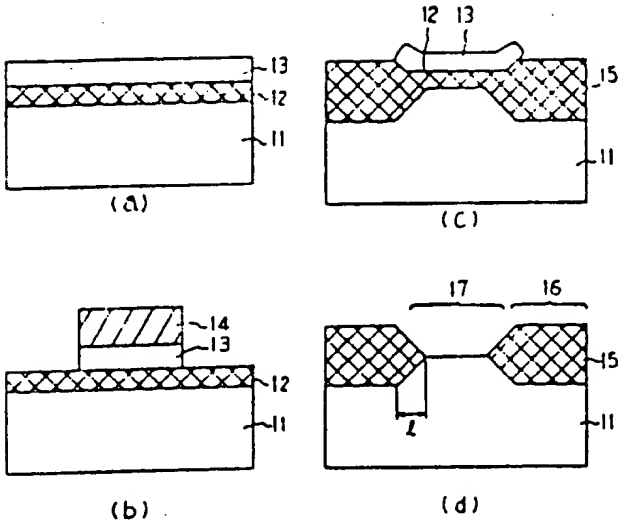
出願人　セイコー電子工業株式会社

代理人　弁理士　最　上　　務（他1名）



本発明の素子分離形成方法の工程順を示す断面図

第1図



従来の素子分離方法の工程順を示す断面図

第2図